MASK DATA PREPARATION

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Field of the Invention

[0001]   The invention relates to the process of fabricating semiconductor chips. More specifically, the invention relates to a method for preparing mask data.

Related Art

[0002]   The high volume manufacturing of integrated circuits relies on the use of optical lithography to define the features printed on the semiconductor chips. The lithography process starts first by coating the surface of the semiconductor wafer with a material called resist. A source of radiation is then shone through the mask in the case of a transparent mask. For a reflective mask the radiation is reflected by the mask. The transparent mask is made of a substrate transparent to the radiation and coated with a patterned opaque layer defining clear and opaque regions to the radiation. Transparent masks are mostly used in optical lithography with typical wavelengths of 436nm, 405nm, 365nm, 248nm, 193nm, and 157nm. The reflective masks are made using a substrate reflective to the radiation and coated with a patterned non-reflective layer defining reflective and non-reflective regions to the radiation. Alternatively, a reflective mask could be made of a non-reflective substrate coated with a reflective layer. Reflective masks are mostly used for shorter radiation wavelength on the order of 13nm usually referred to as EUV or Extreme Ultra Violet.

[0003]   During the exposure to the radiation source, an image of the mask is formed using an optical system on top of the resist layer. Various optical systems can be used to produce an image of the mask. The main technique used today in volume production relies on the projection of the image of the mask onto the wafer. Typically the wafer image is reduced by a factor of 4 (usually named mask image magnification factor or wafer image demagnification factor) as compared to the mask image, thus relaxing the mask fabrication requirements. The field on the wafer corresponding to the image of the

mask is exposed multiple times to cover the entire wafer. The entire field can be exposed in one shot, in this case the equipment is named a stepper.

[0004]   Alternatively, the field can be scanned by moving the mask and the wafer relative to the projection lens. In this case the equipment is named a scanner. Scanners offer the advantage to mitigate some field non-uniformities observed in steppers but the scanning mechanism adds residual noise that partially degrades the aerial image. Moreover scanners show differences of the aerial image for features perpendicular to the scan direction versus features parallel to the scan direction.

[0005]   The resist layer is exposed by the radiation passing through the mask in case of a transparent mask or reflected by the mask in the case of a reflective mask. The resist is then developed in a developer bath and depending on the polarity of the resist (positive or negative), the exposed regions or the unexposed regions of the resist are removed. The end result is a semiconductor wafer with a resist layer having a desired pattern. This resist pattern can then be used by subsequent processing steps of the underlying regions of the wafer.

[0006]   As the feature size decreases, distortion in the pattern transfer process becomes more severe. The design shapes must be modified in order to print the desired images on the wafer. The modifications account for the limitation in the lithography process. One such modification is referred to as Optical Proximity Correction (OPC) in the case of optical lithography. In the case of OPC, modifications of the design image account for optical limitations as well as mask fabrication limitations and resist limitations. Modifications of the design image can also account for the subsequent process steps like dry etching or implantation. It can also account for flare in the optical system as well as pattern density variations. Another application of proximity effect correction is the compensation of the effects of aberrations of the optical system used to print the image of the mask onto the wafers. In this case, a mask with aberration correction would be dedicated to a given lithography tool as the aberrations are tool-specific.

[0007]   Figure 1 illustrates the modification of the mask data to correct for proximity effects. The processing of the mask data starts with a target layout 101 representing the desired dimensions of the image on the wafer. The printed image 102 of

the target layout 101 differs from the desired image due to proximity effect. For reference, the target image 101 is shown with the printed image 102. The edges of the features are then moved (103) so that the corresponding printed image on the wafer 104 is correct (as close to the target as possible). In Figure 1, all the areas of the layout have

5   been corrected but different degrees of proximity effect correction aggressiveness can be applied to different regions depending on the criticality of the region in the integrated circuit.

[0008]   The corrections to layout 101 can be applied using a rule-based approach or a model-based approach. For a rule-based approach (Rule-based OPC), the displacement

10   of the segments would be set by a list of rules depending, for example, on the feature size and its environment. For a model-based approach (Model-based OPC), the printed image on the wafer would be simulated using a model of the pattern transfer process. The correction would be set such that the simulated image matches the desired wafer image. A combination of rule-based OPC and model-based OPC sometimes referred to as hybrid

15   OPC can also be used.

[0009]   In the case of model-based OPC, the original layout 201 as shown in Figure 2 is dissected in smaller segments 203 shown in modified layout 202. Each segment is associated an evaluation point 204. The printed errors of the evaluation points are compensated by moving the corresponding segment in a direction perpendicular to the

20   segment as shown in the final layout 205. The segments are corrected using multiple iterations in order to account for corrections of neighboring segments.

[0010]   The image quality can be improved by adding printing or non-printing assist features along the edges of the main features. These assist features modify the diffraction spectrum of the pattern in a way that improves the printing of the main feature. The

25   practical implementation of assist features is enhanced with the use of proximity effect correction as described above to correct for any optical printing artifact as well as resist and etch artifacts.

[0011]   The image quality can also be improved by using phase-shifting masks. In this case, at least two different regions are created on the masks corresponding to

30   different phase and transmission of the light either going through these regions (for transparent mask) or reflected by these regions (for reflective mask). The phase

difference between the two regions is chosen to be substantially equal to 180 degrees. The destructive interference between adjacent regions of opposite phase creates a very sharp contrast at the boundary between the regions, thus leading to the printing of small features on the wafer. Two main classes of phase-shifting masks are in use today. For the

5 first class, the amount of light transmitted for transparent masks (or reflected for reflective masks) by one region is only a portion of the light transmitted (or reflected) by the other region, typically 5% to 15%. These masks are referred to as attenuated phase-shifting masks or half-tone phase-shifting masks. In some implementation, regions opaque to the light source for transparent mask (with low reflection for reflective masks)

10 are kept on the mask. These types of mask are referred to as tri-tone mask as they have for transparent masks, clear regions, opaque regions, and partially transparent regions (non-reflective, reflective, and partially reflective for reflective masks). For the second class, the light transmitted (for transparent masks) or reflected (for reflective masks) by one region is substantially equal to the light transmitted (for transparent masks) or

15 reflected (for reflective masks) by the other region. The second class of masks includes the following types of phase-shifting masks: alternating aperture phase-shifting masks, chromeless phase-shifting masks, and rim phase-shifting masks. The practical implementation of these techniques is improved with the use of proximity effect correction as described above to correct for any optical printing artifact as well as resist

20 and etch artifacts. All the techniques described in this paragraph can also be combined with the use of assist features.

[0012]   The image quality can also be improved by using off-axis illumination. To achieve off-axis illumination, the illuminator of the stepper or scanner is shaped in a way that only the light at certain angles with respect to the optical axis is used to create the

25 image thereby favoring certain spatial frequencies of the mask pattern. The off-axis setting can be adjusted for a given feature size and type or for a collection of feature sizes and types. Off-axis illumination can be used in combination with binary masks, attenuated phase-shifting masks, chromeless phase-shifting masks, or rim phase-shifting masks. Off-axis illumination will also be improved by the use of proximity effect

30 correction as described in a previous paragraph. Off-axis illumination can also be combined with the use of assist-features.

[0013]   The use of OPC to correct the printing of the features on the wafer has some important implications for mask making. As shown in Figure 2, the data needed to write the mask (205) becomes much more complicated compared to the original data (201). Two main writing strategies are used today for mask manufacturing. For the first strategy named "raster-scan", an electron or optical beam is scanned on the mask and turned on where the mask should be exposed. For the second strategy named "vector-scan", a shaped e-beam is exposed at certain coordinates on the mask representing the data where the mask should be exposed. The shaped beam exposure tools usually require the data to only contain a certain set of angles. Typically these angles are 45 degree, 90 degree and 135 degree angles because of the restriction of the shapes that can be produced by the exposure tool. The complexity of the correction after OPC can create some issue for vector-scan e-beam mask writing tool as very small slivers are created when the data is converted to the mask write tool format as shown in Figure 3. 301 represents the data before OPC, 302 the data after OPC, and 303 the data after fracturing. A sliver 304 was created during the fracturing of the data. These small slivers lead to exposure dose inaccuracies when the mask is exposed which in turn result in dimension inaccuracies.

[0014]   Another issue during the fracturing step is the difficulty to predict the shapes of the polygons created as illustrated in Figure 4. 401 represents the data before OPC, 402 the data after OPC and 403 the data after fracturing. The data 404 represents the same data as 401 rotated by 90 degree clockwise. The data 405 corresponds to the data 404 after OPC. It should be noted that the data 405 can be obtained by rotating by 90 degree clockwise the data 402. The data 406 corresponds to the data 405 after fracturing. In this case 406 cannot be obtained by rotating by 90 degree clockwise the data 403. The fracturing tool does not recognize the fact that the structures 402 and 405 are the same except for a 90-degree clockwise rotation and it creates two outputs 403 and 406 with different fracturing shapes. The difference in fracturing shapes will create some dosage difference between 403 and 406 when the photo-mask is exposed and it will result in dimension errors. This problem can be even more acute in critical areas of the layout. For example, 401 and 404 could represent a portion of a poly level and the dotted line 407 and 408 could represent the corresponding active area. The intersections between 401 and

407 (region 409), and 404 and 408 (region 410), represent the gate regions of the poly level whose dimensions are critical for ensuring the proper operation of the transistors. After fracturing (403 and 406), the regions corresponding to 409 and 410 have been decomposed differently thus creating dimensional difference on the mask because of the

5   nature of the vector scan mask exposure tools.

[0015]   What is needed is a method that prevents the creation of slivers during fracturing. Moreover this method should fracture the same way two same polygons placed with different rotation or mirroring.

10   **Summary**

[0016]   A method for performing proximity effect correction on a layout of an integrated circuit is described. The method consists of fragmenting the polygons of the layout into shapes based upon parameters of a manufacturing tool used for implementing

15   the layout and then performing proximity effect correction on some of the segments of the shapes. The manufacturing tool can be a mask writer or more specifically a vector-scan, e-beam, mask writer. The fragmentation of the shapes can be such that no shape larger than the maximum allowable shape size is created after correction or no shape smaller than the minimum allowable shape size is created after correction.

20   [0017]   This method can also be used to generate the data needed for various types of masks such as binary masks, attenuated phase-shifting masks, tri-tone phase-shifting masks, and alternating phase-shifting masks. In the case of alternating phase-shifting masks, two edges of a given shape may end up abutting two distinct phase-shifting regions and these two regions will need to be out of phase. This information can be stored

25   and used later on when the phase assignment of the shifter regions is performed.

[0018]   In some embodiments, the manufacturing tool is a mask inspection tool.

[0019]   In other embodiments, some edges of the shapes are abutting the boundary of a critical area of the layout. The position of the boundary between the two shapes can also be adjusted to account for the position of the corrected edges of the shapes.

30   [0020]   In some embodiments, polygons within proximity range of a first polygon are taken into account in the fragmentation of the shapes of the first polygon. To facilitate the

fragmentation of the first polygon, corners of the polygons within proximity range can be used.

[0021] Embodiments of the invention include a photolithographic mask. The photolithographic mask comprises a layout pattern that has been corrected for proximity effects using the method described above.

[0022] Embodiments of the invention include a method for manufacturing integrated circuits. The method includes exposing a layer of material in an integrated circuit using a mask defined above. In some embodiments, the polarity of the resist used to define the features on the mask is chosen such that the critical regions of the layout correspond to exposed shapes.

[0023] Embodiments of the invention include a method for producing a photolithographic mask. The photolithographic mask is fabricated using a mask layout. The mask layout includes a layout pattern that has been corrected for proximity effects using the method described above.

[0024] Embodiments of the invention include a system for producing a layout. The system includes a data processor which executes programs of instruction and a memory accessible by the data processor to store programs of instruction. The programs of instruction include logic to receive the computer readable layout of a portion of the integrated circuit and to correct the layout using the correction method described above.

[0025] Embodiments of the invention include an article of manufacture, comprising a machine readable data storage medium storing programs of instruction. The programs of instruction include logic to receive a computer readable layout of a portion of the integrated circuit and to correct the layout using the correction method described above.

[0026] Another method for performing proximity effect correction on a layout is described. The method consists of fragmenting the edges of the polygons of the layout into segments based upon parameters of a manufacturing tool used for implementing the layout and then performing proximity effect correction on some of the segments. Embodiments of the invention include a method for manufacturing integrated circuits. The method includes exposing a layer of material in an integrated circuit using a mask having a mask layout based on the corrected layout described above. In some

embodiments, the polarity of the resist used to define the features on the mask is chosen such that the critical regions of the layout correspond to exposed shapes.

Brief Description of the Figures

[0027]   Figure 1 illustrates the modification of the data to correct proximity effects.

[0028]   Figure 2 illustrates the process flow used for model-based OPC.

[0029]   Figure 3 illustrates the modification of the data to correct proximity effect and to fracture the polygons.

[0030]   Figure 4 compares the OPC and fracturing steps for a polygon oriented at 0 and 90 degrees.

[0031]   Figure 5 depicts a new methodology where the polygons are fractured first and the OPC step is performed next.

[0032]   Figure 6a describes the OPC effects of a maximum inner or outer correction on the shape dimensions.

[0033]   Figure 6b describes the OPC effects on the stitching of the shapes.

[0034]   Figure 7 illustrates the advantage of the invention in terms of preventing the creation of slivers and in terms of reducing the number of shapes created.

[0035]   Figure 8 illustrates the use of polygons in proximity range to define the fracturing of a given polygon.

[0036]   Figure 9 illustrates the notion of shape and the associated edges.

[0037]   Figure 10 illustrates the notion of shape and the associated edges for use in phase-shifting mask.

[0038]   Figure 11 is a block diagram of a computer system adapted for fracturing, proximity effect correction, and verification according to the present invention.

[0039]   Figure 12 is a flow chart for a process of integrated circuit manufacturing according to the present invention.

Detailed Description

[0040]   A technique described in Figure 5 was developed to address the issues encountered during the fracturing of data for vector-scan mask writer. The polygon 501 before correction is first fractured in smaller shapes 502. Some of the edges of the shapes

are abutting the original polygon. During the OPC step, the shapes are modified into 503 and no sliver was created as shown in Figure 5. Fracturing into shapes before OPC presents some important advantages. First, the shapes can be chosen such that even with the largest OPC correction, the shape will not turn into a shape difficult to manufacture

5   for the vector-scan e-beam mask writer. In Figure 6a, 601 represents a shape after fracturing which is a part of a larger polygon 602 (not completely drawn on the figure). During the OPC step, the shape 602 could receive a maximum inner correction or a maximum outer correction as described in Figure 6a. 603 represents the shape after maximum inner correction and 604 represents the shape after maximum outer correction.

10   The advantage of fracturing the shape before OPC as described earlier in Figure 5 is that the dimensions of the shape 601 are chosen such that both cases 603 or 604 can be manufactured reliably using a vector-scan e-beam mask writer. The width of 603 is larger than the minimum width the vector-scan e-beam mask writer can print reliably, i.e. 603 is not a sliver as shown in Figure 3. The width of 604 is smaller than the maximum width

15   the vector-scan e-beam mask writer can print in one single shot, i.e. the shape does not need to be split into two shapes. The fracturing of the shapes can also be optimized for other manufacturing tools besides mask writers like for example mask inspection tools.

[0041]   The use of OPC after fracturing the polygons into shapes will also require the OPC tool to stitch the shapes after correction if needed. Figure 6b shows an example

20   or a corner polygon before correction 605, after fracturing 606, and after OPC 607. The shapes in dotted lines in 607 represent the shapes before OPC, the solid lines represent the shapes after OPC. Note that the original shape 605 was fractured in two shapes 606 containing a 45-degree angle which are valid shapes for the shaped-beam vector-scan mask writer. The advantage of the 45-degree angle in this case (i.e. elbow) is that it

25   minimizes the number of shapes created and facilitates the OPC step. The 45-degree boundary between the two shapes was moved after correction to accommodate for the asymmetric OPC, i.e. the shapes have been stitched back together after OPC. Stitching the shapes is important for shaped-beam vector-scan mask writers as no void can be left between the shapes and no overlap is allowed between the shapes. A void would result in

30   no exposure, an overlap would result in double exposure.

[0042]   Another advantage of fracturing before applying OPC is that the shapes can be chosen such that their edges will follow the edges of critical areas so that during the OPC step, the segments corresponding to critical areas can be corrected with tighter tolerances. For example in Figure 5, 501 can represent a polygon part of the poly level

5   and 504 represents the corresponding active area. The intersection between the polygons 501 and 504 is the gate region which is the critical area of the poly level as explained earlier in reference to Figure 4. It should be noted that this critical area was fractured in exactly two shapes 505 and 506. Some of the edges of the shapes 505 and 506 are abutting the critical area. The two shapes 505 and 506 are converted respectively into the

10   shapes 507 and 508 after OPC. As the shapes 505 and 506 correspond to critical areas of the layout, the tolerance on the correction of these shapes can be made tighter, for example, +/- 1nm maximum edge placement error after correction versus +/- 3nm maximum edge placement error for shapes corresponding to non-critical areas of the layout. Moreover, the number of shapes in the critical regions can be increased compared

15   to non-critical regions in order to achieve a more accurate correction.

[0043]   Another advantage of fracturing before applying OPC is that the shapes can be defined in a way to minimize the total count of shapes and to minimize the chance of creating slivers. Figure 7 shows the example of a polygon 701 (only a portion of the polygon is represented). Using prior art OPC methodology, the polygon 701 is corrected

20   into the polygon 702, which is then fractured into 703. As the edges of the features are independently segmented, any misalignment of the segmentation on the left edge with regard to the right edge can potentially create a sliver during subsequent fracturing as shown on 703. The new method described in this application solves the problem by creating fractured shapes before OPC. The original polygon 704 is fractured into the

25   polygon 705 which is subsequently corrected into the polygon 706. The shapes defined in 705 prevent the issue described in 703. Moreover the total number of shapes can be decreased which in turn will decrease the time it takes to write the mask and the overall cost of manufacturing the mask.

[0044]   Another important aspect of this invention is that the fracturing step can be

30   tailored to the OPC step requirements. In Figure 8, the layout 801 is fractured into the layout 802 and then turned into the layout 803 after OPC. Since the rectangle 804 is

within proximity range of the rectangle 805, its presence will have an impact on the printing of the rectangle 805. Therefore, the corners of the rectangle 804 are used as a reference to create the shape 805 since it is likely that the correction along the edge of the rectangle 805 will be different in the proximity of the rectangle 804. The correction after

5   OPC shows such a difference on the layout 803. If the shape 806 had not been created the correction between the polygons 804 and 805 would have been incorrect. The influence of a corner on an adjacent polygon can be translated into more than one dissection point on the polygon. For more accurate correction, multiple dissection points could be created. Rectangle 804 could belong to the same layer as rectangle 805 or it could belong to a

10   different layer. For example 804 could belong to the active area layer and 805 could belong to the gate layer.

[0045]   Figures 5, 6, 7, and 8 emphasize the need to combine OPC parameters and fracturing parameters. For example the segmentation performed during the OPC step need to be consistent with the segmentation done at fracturing. The usual flow of

15   fracturing the data after performing OPC can also be improved if the OPC parameters are chosen in such a way that they do not create any issue with the subsequent fracturing step. The advantage of fracturing first (i.e. before the OPC step) is that the shapes are defined first and the creation of small slivers as described in Figure 5 can be avoided by making sure that the shape dimension is compatible with the maximum OPC correction

20   (described in Figure 6a).

[0046]   At the layout stage of an integrated circuit, the data is represented in a hierarchical fashion in order to minimize the amount of data needed to describe the circuitry. The hierarchical tree obtained is made of cells containing data and placement of other cells. To implement this technique hierarchical fracturing will be required. One of

25   the hurdles to the implementation of hierarchical fracturing is the need for partitioning the layout into fields required by the vector-scan e-beam mask writers. At the boundaries of these fields, or for some mask writer in the vicinity of the boundaries, the polygons should be cut. Preferably, two placements of a cell in two different environments with a different fracturing boundary will have to be named differently since the fracturing result

30   of the cell could be different.

[0047]   Depending on the resist used to fabricate the mask, the layout data or a reverse-tone image of the layout data will be needed. If the layout data represents areas of the mask that should be dark, the layout data can be fractured directly to expose the mask with a negative-tone resist. On the other hand, the reverse-tone image of the layout data

5   will be needed to expose the mask with a positive tone resist. If the layout data represents areas of the mask that should be clear (quartz), the layout data can be fractured directly to expose the mask with a positive-tone resist. On the other hand, the reverse-tone image of the layout data will be needed to expose the mask with a negative tone resist. The technique of this invention works for both cases. Preferably the resist polarity used to

10   fabricate the mask will be chosen to minimize the volume of data, i.e. the number of shapes. For better dimension control, the resist polarity should be chosen in such a way that the critical dimensions of the layout are defined by exposed shapes. For example, in Figure 5, a negative tone resist should be used to manufacture the mask to obtain a dark (chrome) 503 representation. If a positive tone resist were used the data volume would

15   considerably increase (the complementary of data 503 would be exposed). Since the regions outside of data 503 are exposed, the size and dimensions of the shapes needed to expose the mask would depend on adjacent patterns. It would therefore be impossible to predict the shapes needed to create the critical gate regions thus creating possible dimensional control issue. On the other hand 507 and 508 clearly define the gate region

20   for a negative-tone resist in this specific example thus ensuring a better control of the exposure of the gate region independently of its environment.

[0048]   The approach described in Figure 5 emphasizes the need for a shape-based data processing engine. Shapes are created before any data processing is performed. Figure 9 describes how the shapes can be used for subsequent processing steps. A shape

25   902 is shown in polygon 901. A magnified view of the shape is given on the right side of Figure 9. The shape can be decomposed in two types of edges, edges that will create a printed edge on the wafer (903) and edges that will not create a printed edge on the wafer (904, 905, 906). All edges (903, 904, 905, 906) are important for the fracturing step as they are all required to define the shape. For OPC, only the edges creating printed edges

30   on the wafer are important (903) as the position of the printed edge is being corrected to reflect the original layout. The data can also be verified to make sure that the printed edge

is at the location defined in the original layout. In this case, only the edges creating printed edges on the wafer are important (903).

[0049]   The conversion of the data for phase-shifting mask can also be handled using the concept of shapes. In this case, only edges of the shapes resulting in printing edges will be important. Additional information can be used if two edges of a given shape result in the printing of opposite edges of a feature that need to be phase-shifted. Figure 10 describes how the shapes can be used for phase-shifting the layout. A shape 1002 is shown in polygon 1001. A magnified view of the shape is given on the right side of Figure 10. As for Figure 10, the shape can be decomposed in two types of edges, edges that will create a printed edge on the wafer (1003 and 1005) and edges that will not create a printed edge on the wafer (1004,1006). For a phase-shifting mask, edge 1003 and 1005 are adjacent to a shifter region. To create the desired phase-shifting effect, the shifter region adjacent to edge 1003 should be out of phase of the shifter region adjacent to edge 1005. The information about the edges 1003 and 1005 can be stored and later on used to assign the phase of the phase-shifting regions.

[0050]   Figure 11 illustrates a computer system that can be used to fracture the data, applying OPC and verifying the data. This computer system represents a wide variety of computer systems and computer architectures suitable for this application. A processor 1101 is connected to receive data indicating user signals from user input device 1102 and to provide data defining images to display 1103. Processor 1101 is also connected for accessing mask layout data 1104, which define a mask layout under construction and a layout for a layer of material to be exposed using the mask. Processor 1101 is also connected for receiving instruction data from instruction input device 1105, which can provide instructions received from connections to memory 1106, storage medium access device 1107, or network 1108.

[0051]   Figure 12 illustrates the manufacturing process of an IC (Integrated Circuit). At step 1201, the layout file of the integrated circuit is first read using a computer system described in Figure 11. At step 1202, the layout is fractured and then corrected for proximity effect. The data resulting from step 1202 is used to create a mask at step 1203, and the mask is finally used in the fabrication process of an IC at step 1204.

[0052]   The technique described above can also be used to directly create an image on the wafer using tools referred to as "direct-write" tools. The direct-write tool could be an optical tool, an e-beam tool, or and EUV tool. In this case the OPC step would be replaced by a step including the correction of the proximity effects created by the direct write tool.

Conclusion

[0053]   The data structures and code described in this description can be stored on a computer readable storage medium, which may be any device or medium that can store code and/or data for use by a computer system. This includes, but is not limited to, magnetic and optical storage devices such as disk drives, magnetic tapes, CD (compact discs) and DVD (digital video disks), and computer instruction signals embodied in a transmission medium. For example, the transmission medium may include a communication network, such as the Internet.

[0054]   The invention can be applied to any binary masks, rim phase-shifting masks, chromeless phase-shifting masks, attenuated phase-shifting masks, alternating aperture phase-shifting masks used in single or multiple exposure methodologies.

[0055]   While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will readily occur to those skilled in the art, which modifications and combinations will be within the spirit of the invention and the scope of the following claims. What is claimed is: